X1830

IoT Application Processor

Data Sheet

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Disclaimer

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1 Overview

X1830 is a IoT application processor targeting for smart multimedia devices like smart speaker, security survey, video talking, video analysis and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB L2 cache, operating at 1.5GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included. The MXU2.0(SIMD128) instruction set has been implemented by XBurst® engine, and is one part of the CPU.

With the powerful CPU, X1830 supports various computer vision applications, such as face detection, human detection, gesture recognition, and etc. Also people can develop new computer vision application using the MXU2.0 to accelerate it.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. Together with the on chip video accelerating engine and post processing unit, X1830 delivers high video performance. The maximum resolution of 1560x1600 in the format of H.264 are supported in encoding. up to 50Mbit/s, 1080P@80fps.

The ISP (Image signal processor) core supports excellent image process with the image from raw sensors. It supports DVP MIPI CSI-2 and LVDS interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2688x2048 resolution image for view or encoding to store or transfer.

For more quickly and easily to use X1830, 1024Mbit DDR2 is integrated.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

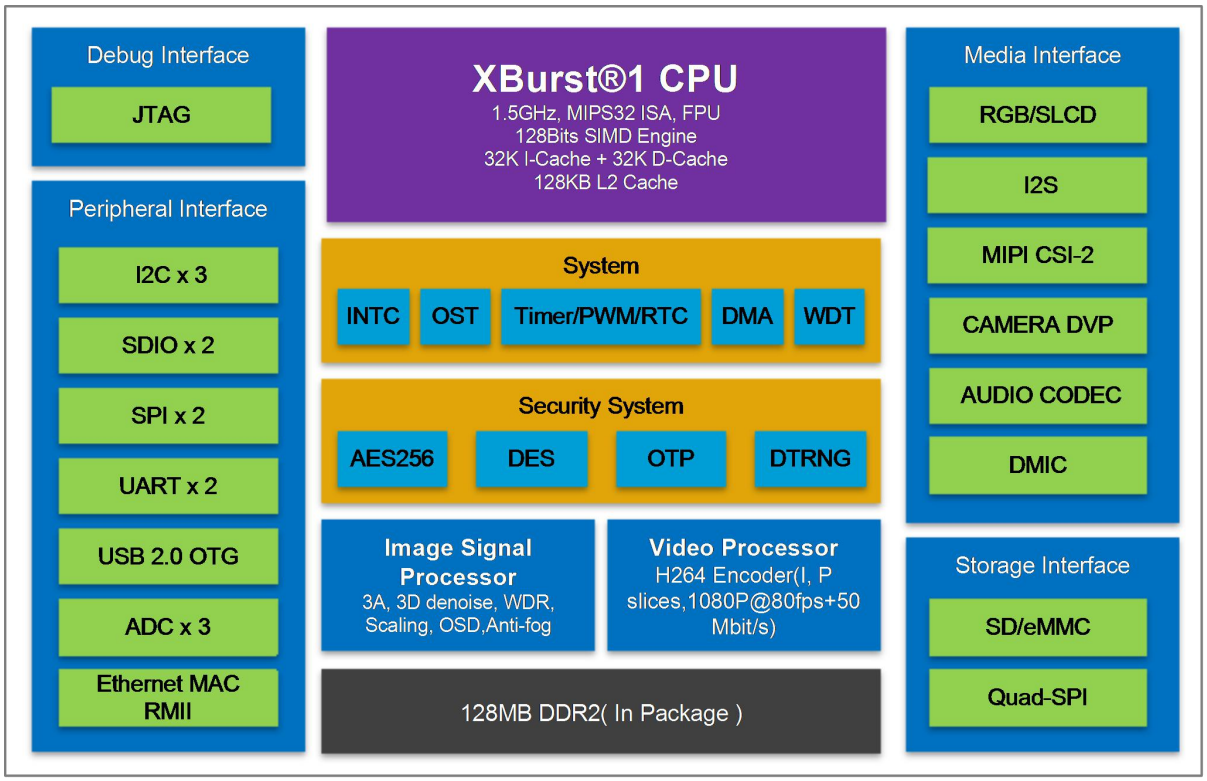


Figure 1-1 X1830 Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
  - XBurst® RISC instruction set
  - XBurst® SIMD128 instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.5GHz
- MMU
  - 32-entry joint-TLB
  - 8-entry Instruction TLB
  - 8-entry data TLB
- L1 Cache
  - 32KB instruction cache
  - 32KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unified cache

1.2.2 VPU

- Support H264 Encoder(I、P slices)
- Support H264 baseline main high profile encoding up to 50Mbit/s, 1080P@80fps
- Support H264 maximum size up to 1560x1600 resolution
- Only support JZ-bitstream Decoder
- JPEG compressing/decompressing up to 70Mega-pixels per second（baseline）

1.2.3 ISP

- Output support two channel: FR is 2688x2048 @20fps, DS1 is 1080p @60fps
- The Module support Max input resolution 2688x2048 @20fps, 1080p @60fps,720p @120fps
- Input image up to 12bit RAW or Up to 24bit RGB. Both RGB and YCbCr are supported from sensor
- Up to 2 output channel. Image crop and downscaler
- 2-D and 3-D noise reduction filter lead to high levels of noise reduction with minimal effect on edges and textures
- Single frame and multi frame WDR/HDR provide high dynamic range in both still and video capture modes
- Advanced demosaic, color processing, lens shading, defog, glare, static/dynamic defect pixel and other modules provide high image quality
- 3A supported
- Flash timer

1.2.4 Image post processor(IPU)

- DMA mode for data transaction, Input format:
  - Input data format: ARGB,RGB,NV12/NV21
  - Output data format: ARGB,RGB,NV12/NV21,HSV
- Color conversion feature: input and output format can be chosen freely from input and output data format.
- Minimum input image size (pixel): 4x4
- Maximum input image size (pixel): 2592x2048
- Minimum output image size (pixel): 4x4
- Maximum output image size (pixel): 2592x2048
- Background channel OSD function:
  - Support 4 layers OSD
  - Support whole background picture into OSD process and partial picture into OSD process
  - Support 12 port-duff OSD modes
  - Support 5 input format in background channel: ARGB8888, ARGB1555, RGB888, NV12, NV21. RGB can be in following sequence: RGB, RBG, BRG, BGR, GRB, GBR. Specifically, RGB888 format data occupy 4 bytes when stored in memory, RGB occupy three bytes, and the forth byte can be any value.

- Output picture format must be the same with the input picture format of separated background channel.

1.2.5 Display (LCD)

- Layer feature
  - Support 2 layer DMA channel
  - Support input format：RGB8888/888/565/555,NV12/NV21
  - Support frame size 4x4~800x800
  - Support global alpha
- Composition feature
  - Support 2 layer Alpha Blending
  - Support frame size 4x4~800x800
- Display feature
  - Support TFT(RGB666)
  - Support SLCD
  - Support 640x480@60hz

1.2.6 Video input

- Support 8/10/12 bit RGB Bayer input
- Support maximum：2688x2048 @20fps, 1080p @60fps,720p @120fps
- Support single-sensor input
- Support DVP/BT1120
- Support MIPI CSI2 2-lane
- Support LVDS IEEE Std1596.3-1996

1.2.7 Audio

- Integrated Audio codec.
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K

1.2.8 Memory Interface

- Integrated 1024Mbits DDR2
- Static memory interface

- Support 6 external chip selection CS6~1#. Each bank can be configured separately
- The size and base address of static memory banks are programmable
- Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
- Wait insertion by WAIT pin
- Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

1.2.9 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - One four-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock
  - MSC clock supports 100M clock
  - Functional-unit clock gating
  - Shut down power supply for P0, ISP, VPU, IPU, LCD, LDC
- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset

  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - 3 Channels
  - Resolution: 10-bit
  - Integral nonlinearity: ±1 LSB
  - Differential nonlinearity: ±0.5 LSB
  - Resolution/speed: up to 2MSPS
  - Max Frequency: 24MHz
  - Low power dissipation: 1.5mW(worst)
  - Support multi-touch detect
  - Support write control command by software
  - Single-end and Differential Conversion Mode
  - Support external touch screen controller
  - Pin Description
- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
- OTP Slave Interface
  - Total 1024 bits. Lower 192bits are read only, other higher bits are read-able and write-able

1.2.10 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge

triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 4 interrupts, each interrupt corresponds to the group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 3 independent SMB channels (SMB0, SMB1, SMB2)
- One High Speed Synchronous serial interfaces (SFC)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - transmit-only or receive-only operation
  - MSB first for command and data transfer, and LSB first for address transfer
  - 64 entries x 32 bits wide data FIFO
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: tSLCH, tCHSH and tSHSL
  - Configurable flash address wide are supported
  - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow
- Two Normal Speed Synchronous serial interfaces (SSI0, SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing

- Two UARTs (UART0, UART1)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer
- Digital True Random Number Generator（DTRNG）

- Pure digital logic circuits
- True random number
- Interrupt mode and no interrupt mode

1.2.11 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	28nm CMOS low power
Power supply voltage	General purpose I/O: 1.5~3.6V DDR I/O for DDR2: 1.8V ± 0.1V RTC I/O: 1.5V~3.6V EFUSE programming: 1.5V ± 10% Analog power supply 1: 1.8V ± 10% Analog power supply 2: 3.3V ± 10% Core supply: 1.3V ± 0.1V
Package	BGA223 11mm x 11mm x 1.22mm, 0.65mm pitch
Operating frequency	1.5 GHz

2 Packaging and Pinout Information

2.1 Overview

X1830 processor is offered in 223-pin BGA package, which is 11mm x 11mm x 1.22mm outline, 17 x 17 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The X1830 pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1 ~ Table 2-18.

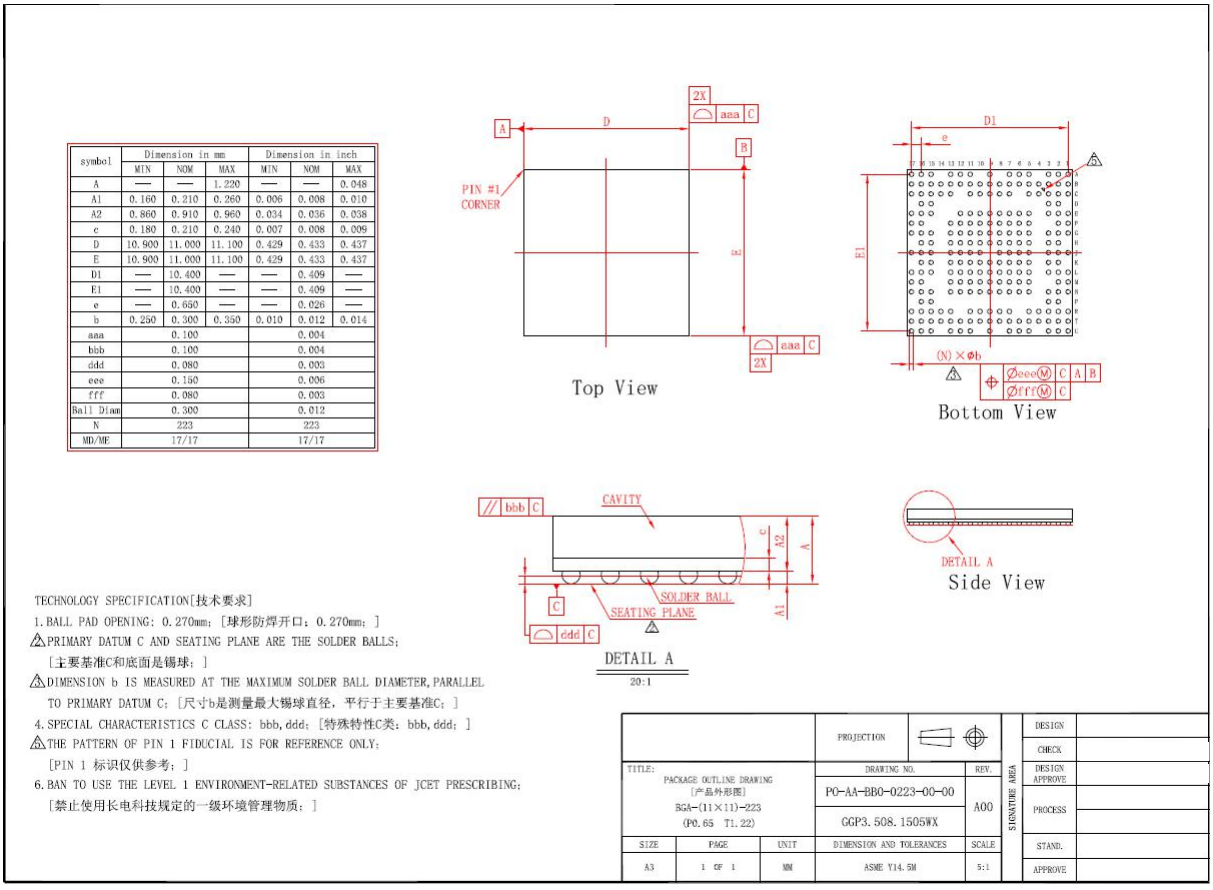
2.2 Solder Process

X1830 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

X1830 package moisture sensitivity is level 3.

2.4 X1830 Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.220	—	—	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.180	0.210	0.240	0.007	0.008	0.009
D	10.900	11.000	11.100	0.429	0.433	0.437
E	10.900	11.000	11.100	0.429	0.433	0.437
D1	—	10.400	—	—	0.409	—
E1	—	10.400	—	—	0.409	—
e	—	0.650	—	—	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	223			223		
MD/ME	17/17			17/17		

Figure 2-1 X1830 package outline drawing

Figure 2-2 X1830 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DVP/I2C0

Table 2-1 DVP/I2C0 Pins(12)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DVP_D6 PA06	I IO	T13	8mA	DVP_D6:DVP data bit 6 PA06: GPIO group A bit 06	VDDIO_D

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DVP_D7 PA07	I IO	U15	8mA	DVP_D7:DVP data bit 7 PA07: GPIO group A bit 07	VDDIO_D
DVP_D8 PA08	I IO	T14	8mA	DVP_D8:DVP data bit 8 PA08: GPIO group A bit 08	VDDIO_D
DVP_D9 PA09	I IO	R13	8mA	DVP_D9:DVP data bit 9 PA09: GPIO group A bit 09	VDDIO_D
DVP_D10 PA10	I IO	U16	8mA	DVP_D10:DVP data bit 10 PA10: GPIO group A bit 10	VDDIO_D
DVP_D11 PA11	I IO	T15	8mA Pullup-rst	DVP_D11:DVP data bit 11 PA11: GPIO group A bit 11	VDDIO_D
SMB0_SDA PA12	IO IO	R9	8mA Pullup-rst	SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO_D
SMB0_SCK PA13	IO IO	U9	8mA Pullup-rst	SMB0_SCK: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO_D
DVP_PCLK PA14	I IO	T12	8mA	DVP_PCLK: camera sensor clock input PA14: GPIO group A bit 14	VDDIO_D
DVP_MCLK PA15	O IO	U13	8mA Slew-rate-rst	DVP_MCLK: DVP clock output PA15: GPIO group A bit 15	VDDIO_D
DVP_HSYNC PA16	I IO	U12	8mA	DVP_HSYNC: DVP horizontal sync PA16: GPIO group A bit 16	VDDIO_D
DVP_VSYNC PA17	I IO	R11	8mA	DVP_VSYNC: DVP vertical sync PA17: GPIO group A bit 17	VDDIO_D

NOTES:

1. DVP data bit0~5 reused with MIPI CSI.

2.5.2 SFC

Table 2-2 SFC Pins(6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SFC_DT PA23	IO IO	R8	8mA Pullup-rst	SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23	VDDIO
SFC_DR PA24	IO IO	U7	8mA Pullup-rst	SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24	VDDIO
SFC_GPC PA25	IO IO	T9	8mA Pullup-rst	SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25	VDDIO
SFC_CE1 PA26	IO IO	T7	8mA Pullup-rst	SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26	VDDIO
SFC_CLK PA27	IO IO	T8	8mA Pullup-rst	SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27	VDDIO
SFC_CE0 PA28	IO IO	R7	8mA Pullup-rst	SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28	VDDIO

2.5.3 Static Memory/MSC0/GMAC/PWMx/UARTx/I2C1/JTAG

Table 2-3 Static Memory/MSC0/GMAC/PWMx/UARTx/I2C1/JTAG (26)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 SD0 PB00	IO IO IO	E15	8mA	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SD0: Static memory data bus bit 0 PB00: GPIO group B bit 00	VDDIO
MSC0_D1 SD1 PB01	IO IO IO	E16	8mA	MSC0_D1: MSC (MMC/SD) 0 data bit 1 SD1: Static memory data bus bit 1 PB01: GPIO group B bit 01	VDDIO
MSC0_D2 SD2 PB02	IO IO IO	C16	8mA	MSC0_D2: MSC (MMC/SD) 0 data bit 2 SD2: Static memory data bus bit 2 PB02: GPIO group B bit 02	VDDIO
MSC0_D3 SD3 PB03	IO IO IO	C17	8mA	MSC0_D3: MSC (MMC/SD) 0 data bit 3 SD3: Static memory data bus bit 3 PB03: GPIO group B bit 03	VDDIO
MSC0_CLK SD4 PB04	O IO IO	D16	8mA	MSC0_CLK: MSC (MMC/SD) 0 clock output SD4: Static memory data bus bit 4 PB04: GPIO group B bit 04	VDDIO
MSC0_CMD SD5 PB05	IO IO IO	D15	8mA	MSC0_CMD: MSC (MMC/SD) 0 command SD5: Static memory data bus bit 5 PB05: GPIO group B bit 05	VDDIO
GMAC_TXCLK SD6 PB06	I IO IO	R5	8mA	GMAC_TXCLK: gmac transmitting clock SD6: Static memory data bus bit 6 PB06: GPIO group B bit 06	VDDIO
GMAC_PHY_CLK SD7 PB07	O IO IO	T5	8mA	GMAC_PHY_CLK: gmac phy clock SD7: Static memory data bus bit 7 PB07: GPIO group B bit 07	VDDIO
GMAC_TXEN PB08	O IO	U6	8mA	GMAC_TXEN: gmac transmitting enable PB08: GPIO group B bit 08	VDDIO
GMAC_RXDV PB09	I IO	U3	8mA	GMAC_RXDV: gmac receive data valid PB09: GPIO group B bit 09.	VDDIO
GMAC_MDCK PB10	O IO	T3	8mA Pulldown-rst	GMAC_MDCK: gmac manage data clock PB10: GPIO group B bit 10.	VDDIO
GMAC_MDIO PB11	IO IO	U2	8mA Pullup-rst	GMAC_MDIO: gmac MDIO which is clocked by MDC PB11: GPIO group B bit 11.	VDDIO
GMAC_TXD0 SA0 PB13	O O IO	U5	8mA	GMAC_TXD0: gmac transmit data bit 0 SA0: Static memory address bus bit 0 PB13: GPIO group B bit 13.	VDDIO
GMAC_TXD1 SA1 PB14	O O IO	T6	8mA	GMAC_TXD1: gmac transmit data bit 1 SA1: Static memory address bus bit 1 PB14: GPIO group B bit 14.	VDDIO
GMAC_RXD0 SA2 PB15	I O IO	R4	8mA	GMAC_RXD0: gmac receive data bit 0 SA2: Static memory address bus bit 2 PB15: GPIO group B bit 15.	VDDIO
GMAC_RXD1 PB16	I IO	T4	8mA	GMAC_RXD1: gmac receive data bit 1 PB16: GPIO group B bit 16.	VDDIO
PWM0 PB17	O IO	A5	8mA Pulldown-rst	PWM0: PWM channel 0 output signal PB17: GPIO group B bit 17.	VDDIO
PWM1 CLK32K_OUT PB18	O O IO	A6	8mA Pulldown-rst	PWM1: PWM channel 1 output signal CLK32K_OUT: 32.768K clock output PB18: GPIO group B bit 18.	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RXD TDI PB19	I I IO	A17	8mA Pullup-rst	UART0_RXD: UART 0 receive data TDI: JTAG data input PB19: GPIO group B bit 19	VDDIO
UART0_CTS PB20	I IO	B16	8mA	UART0_CTS: UART 0 Clear-to-Send handshaking signal PB20: GPIO group B bit 20	VDDIO
UART0_RTS PB21	O IO	A16	8mA	UART0_RTS: UART 0 Request-to-Send handshaking signal PB21: GPIO group B bit 21	VDDIO
UART0_TXD TDO PB22	O O IO	B15	8mA	UART0_TXD: UART 0 transmit data TDO: JTAG data output PB22: GPIO group B bit 22	VDDIO
UART1_TXD TCK PB23	O I IO	A15	8mA	UART1_TXD: UART 1 transmit data TCK: JTAG clock input PB23: GPIO group B bit 23	VDDIO
UART1_RXD TMS CS1 PB24	I I O IO	C14	8mA Pullup-rst	UART1_RXD: UART 1 receive data TMS: JTAG mode select CS1: Static memory chip 1 select PB24: GPIO group B bit 24	VDDIO
SMB1_SDA CS2 PB25	IO O IO	B17	8mA Pullup-rst	SMB1_SDA: I2C 1 serial data CS2: Static memory chip 2 select PB25: GPIO group B bit 25	VDDIO
SMB1_SCK RD PB26	IO O IO	C15	8mA Pullup-rst	SMB1_SCK: I2C 1 serial clock RD: Static memory read PB26: GPIO group B bit 26	VDDIO

2.5.4 MSC1/PWMx/SSIx/I2S/DMIC/CAMERA/I2C2

Table 2-4 MSC1/PWMx/SSIx/I2S/DMIC/CAMERA/I2C2 Pins (26)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_CLK PC02	O IO	B2	8mA	MSC1_CLK: MSC (MMC/SD) 1 clock output PC02: GPIO group C bit 02	VDDIO
MSC1_CMD PC03	IO IO	B1	8mA	MSC1_CMD: MSC (MMC/SD) 1 command PC03: GPIO group C bit 03	VDDIO
MSC1_D0 PC04	IO IO	A1	8mA	MSC1_D0: MSC (MMC/SD) 1 data bit 0 PC04: GPIO group C bit 04	VDDIO
MSC1_D1 PC05	IO IO	C3	8mA	MSC1_D1: MSC (MMC/SD) 1 data bit 1 PC05: GPIO group C bit 05	VDDIO
MSC1_D2 PC06	IO IO	C1	8mA	MSC1_D2: MSC (MMC/SD) 1 data bit 2 PC06: GPIO group C bit 06	VDDIO
MSC1_D3 PC07	IO IO	C2	8mA	MSC1_D3: MSC (MMC/SD) 1 data bit 3 PC07: GPIO group C bit 07	VDDIO
PWM2 FLASH_STORBE_IN DMIC_CLK PC08	O I O IO	B6	8mA Pulldown-rst Schmitt-rst	PWM2: PWM channel 2 output signal FLASH_STORBE_IN: camera flash store input DMIC_CLK: digital microphone clock output PC08: GPIO group C bit 08.	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM3 FLASH_OUT PC09	O O IO	A7	8mA Pulldown-rst Schmitt-rst	PWM3: PWM channel 3 output signal FLASH_OUT: camera flash out signal PC09: GPIO group C bit 09.	VDDIO
SSI0_DR PWM0 PC11	I O IO	B10	8mA	SSI0_DR: normal speed ssi 0 receive data PWM0: PWM channel 0 output signal PC11: GPIO group C bit 11.	VDDIO
SSI0_DT PWM1 PC12	O O IO	C10	8mA	SSI0_DT: normal speed ssi 0 transmit data PWM1: PWM channel 1 output signal PC12: GPIO group C bit 12.	VDDIO
SSI0_GPC PWM2 PC13	O O IO	A11	8mA	SSI0_GPC: normal speed ssi 0 general-purpose control PWM2: PWM channel 2 output signal PC13: GPIO group C bit 13.	VDDIO
SSI0_CE1 PWM3 PC14	O O IO	A9	8mA	SSI0_CE1: normal speed ssi 0 chip 1 select PWM3: PWM channel 3 output signal PC14: GPIO group C bit 14.	VDDIO
SSI0_CLK PWM4 PC15	O O IO	B11	8mA	SSI0_CLK: normal speed ssi 0 clock PWM4: PWM channel 4 output signal PC15: GPIO group C bit 15.	VDDIO
SSI0_CE0 PWM5 PC16	O O IO	C11	8mA Pullup-rst	SSI0_CE0: normal speed ssi 0 chip 0 select PWM5: PWM channel 5 output signal PC16: GPIO group C bit 16.	VDDIO
DRV_VBUS PWM6 PC17	O O IO	E3	8mA	DRV_VBUS:USB-5V control signal PWM6: PWM channel 6 output signal PC17: GPIO group C bit 17.	VDDIO
I2S_DAC_LRCK PWM7 PC18	IO O IO	A2	8mA Schmitt-rst	I2S_DAC_LRCK: I2S DAC left/right clock PWM7: PWM channel 7 output signal PC18: GPIO group C bit 18.	VDDIO
I2S_SDTO SSI1_DT PC19	O O IO	B3	8mA Schmitt-rst	I2S_SDTO: I2S serial data output signal SSI1_DT: normal speed ssi 1 transmit data PC19: GPIO group C bit 19.	VDDIO
I2S_SDTI SSI1_DR PC20	I I IO	A3	8mA	I2S_SDTI:I2S serial data input signal SSI1_DR: normal speed ssi 1 receive data PC20: GPIO group C bit 20.	VDDIO
I2S_ADC_LRCK SSI1_GPC PC21	O O IO	B4	8mA	I2S_ADC_LRCK: I2S ADC left/right clock SSI1_GPC: normal speed ssi 1 general-purpose control PC21: GPIO group C bit 21.	VDDIO
I2S_ADC_BCLK SSI1_CE1 PC22	IO O IO	C4	8mA	I2S_ADC_BCLK: I2S ADC bit clock SSI1_CE1: normal speed ssi 1 chip 1 select PC22: GPIO group C bit 22.	VDDIO
I2S_MCLK SSI1_CLK PC23	O O IO	C5	8mA	I2S_MCLK: I2S system clock SSI1_CLK: normal speed ssi 1 clock PC23: GPIO group C bit 23.	VDDIO
I2S_DAC_BCLK SSI1_CE0 WAIT PC24	IO O I IO	B5	8mA Pullup-rst Schmitt-rst	I2S_DAC_BCLK: I2S DAC bit clock SSI1_CE0: normal speed ssi 1 chip 0 select WAIT: Slow static memory/device wait signal PC24: GPIO group C bit 24.	VDDIO
PWM4 DMIC_DAT0 PC25	O I IO	B7	8mA Pulldown-rst	PWM4: PWM channel 4 output signal DMIC_DAT0: digital microphone data bit 0 PC25: GPIO group C bit 25.	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM5 DMIC_DAT1 PC26	O I IO	C7	8mA Pulldown-rst	PWM5: PWM channel 5 output signal DMIC_DAT1: digital microphone data bit 1 PC26: GPIO group C bit 26.	VDDIO
PWM6 SMB2_SDA PC27	O IO IO	B8	8mA Pulldown-rst	PWM6: PWM channel 6 output signal SMB2_SDA: I2C 2 serial data PC27: GPIO group C bit 27.	VDDIO
PWM7 SMB2_SCK PC28	O IO IO	C8	8mA Pulldown-rst	PWM7: PWM channel 7 output signal SMB2_SCK: I2C 2 serial clock PC28: GPIO group C bit 28.	VDDIO

2.5.5 LCD/SSI1

Table 2-5 LCD/SSI1 Pins (22)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TFT_D2 SLCD_D0 SSI1_DT PD02	O O O IO	N15	8mA	TFT_D2: TFT data output bit 2SLCD_D0: smart lcd data output bit 0 SSI1_DT: normal speed ssi 1 transmit data PD02: GPIO group D bit 02.	VDDIO
TFT_D3 SLCD_D1 SSI1_DR PD03	O O I IO	P16	8mA	TFT_D3: TFT data output bit 3 SLCD_D1: smart lcd data output bit 1 SSI1_DR: normal speed ssi 1 receive data PD03: GPIO group D bit 03.	VDDIO
TFT_D4 SLCD_D2 SSI1_GPC PD04	O O O IO	N16	8mA	TFT_D4: TFT data output bit 4 SLCD_D2: smart lcd data output bit 2 SSI1_GPC: normal speed ssi 1 general-purpose control PD04: GPIO group D bit 04.	VDDIO
TFT_D5 SLCD_D3 SSI1_CE1 PD05	O O O IO	N17	8mA	TFT_D5: TFT data output bit 5 SLCD_D3: smart lcd data output bit 3 SSI1_CE1: normal speed ssi 1 chip 1 select PD05: GPIO group D bit 05.	VDDIO
TFT_D6 SLCD_D4 SSI1_CLK PD06	O O O IO	M16	8mA	TFT_D6: TFT data output bit 6 SLCD_D4: smart lcd data output bit 4 SSI1_CLK: normal speed ssi 1 clock PD06: GPIO group D bit 06.	VDDIO
TFT_D7 SLCD_D5 SSI1_CE0 PD07	O O O IO	M17	8mA Pullup-rst	TFT_D7: TFT data output bit 7 SLCD_D5: smart lcd data output bit 5 SSI1_CE0: normal speed ssi 1 chip 0 select PD07: GPIO group D bit 07.	VDDIO
LCD_PCLK PD08	O IO	L16	8mA	LCD_PCLK: lcdc pixel clock output PD08: GPIO group D bit 08.	VDDIO
TFT_DE SLCD_WR PD09	O O IO	K16	8mA	TFT_DE: TFT data enable signal SLCD_WR: smart lcd write data control signal PD09: GPIO group D bit 09.	VDDIO
TFT_D10 SLCD_D6 PD12	O O IO	J17	8mA	TFT_D10: TFT data output bit 10 SLCD_D6: smart lcd data output bit 6 PD12: GPIO group D bit 12.	VDDIO
TFT_D11 SLCD_D7	O O	J16	8mA	TFT_D11: TFT data output bit 11 SLCD_D7: smart lcd data output bit 7	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD13	IO			PD13: GPIO group D bit 13.	
TFT_D12 SLCD_D8 PD14	O O IO	K15	8mA	TFT_D12: TFT data output bit 12 SLCD_D8: smart lcd data output bit 8 PD14: GPIO group D bit 14.	VDDIO
TFT_D13 SLCD_D9 PD15	O O IO	G17	8mA	TFT_D13: TFT data output bit 13 SLCD_D9: smart lcd data output bit 9 PD15: GPIO group D bit 15.	VDDIO
TFT_D14 SLCD_D10 PD16	O O IO	H16	8mA	TFT_D14: TFT data output bit 14 SLCD_D10: smart lcd data output bit 10 PD16: GPIO group D bit 16.	VDDIO
TFT_D15 SLCD_D11 PD17	O O IO	J15	8mA	TFT_D15: TFT data output bit 15 SLCD_D11: smart lcd data output bit 11 PD17: GPIO group D bit 17.	VDDIO
TFT_VSYNC SLCD_CS PD18	O O O	L17	8mA Pullup-rst	TFT_VSYNC:TFT column sync SLCD_CS: smart lcd chip select signal PD18: GPIO group D bit 18.	VDDIO
TFT_HSYNC SLCD_TE PD19	O I IO	L15	8mA	TFT_HSYNC:TFT horizontal sync SLCD_TE: smart lcd crack control signal PD19: GPIO group D bit 19.	VDDIO
TFT_D18 SLCD_D12 PD22	O O IO	F17	8mA	TFT_D18: TFT data output bit 18 SLCD_D12: smart lcd data output bit 12 PD22: GPIO group D bit 22.	VDDIO
TFT_D19 SLCD_D13 PD23	O O IO	G16	8mA	TFT_D19: TFT data output bit 19 SLCD_D13: smart lcd data output bit 13 PD23: GPIO group D bit 23.	VDDIO
TFT_D20 SLCD_D14 PD24	O O IO	E17	8mA	TFT_D20: TFT data output bit 20 SLCD_D14: smart lcd data output bit 14 PD24: GPIO group D bit 24.	VDDIO
TFT_D21 SLCD_D15 PD25	O O IO	F16	8mA	TFT_D21: TFT data output bit 21 SLCD_D15: smart lcd data output bit 15 PD25: GPIO group D bit 25.	VDDIO
TFT_D22 SLCD_RDY PD26	O O IO	H15	8mA	TFT_D22: TFT data output bit 22 SLCD_RDY: smart lcd work status signal PD26: GPIO group D bit 26.	VDDIO
TFT_D23 SLCD_DC PD27	O O IO	G15	8mA	TFT_D23: TFT data output bit 23 SLCD_DC: smart lcd cmd/data identify signal PD27: GPIO group D bit 27.	VDDIO

2.5.6 GPIO

Table 2-6 GPIO Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PA18	IO	T10	8mA	PA18: GPIO group A bit 18	VDDIO_D
PA19	IO	U11	8mA Schmitt-rst	PA19: GPIO group A bit 19	VDDIO_D
PA20	IO	T11	8mA	PA20: GPIO group A bit 20	VDDIO_D

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
			Schmitt-rst		
PA22	IO	R10	8mA Pullup-rst Schmitt-rst	PA22: GPIO group A bit 22	VDDIO_D
PB27	IO	A13	8mA Schmitt-rst	PB27: GPIO group B bit 27	VDDIO
PB28	IO	B13	8mA Schmitt-rst	PA28: GPIO group B bit 28	VDDIO
PB29	IO	C13	8mA Schmitt-rst	PB29: GPIO group B bit 29	VDDIO
PB30	IO	B12	8mA Schmitt-rst	PB30: GPIO group B bit 30	VDDIO
PB31	IO	A12	8mA Pulldown-rst	PB31: GPIO group B bit 31	VDDIO

2.5.7 System

Table 2-7 System Control Pins(6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST	I	B14	8mA Schmitt Pull-down	TRST: JTAG reset	VDDIO
RST_OUT	O	G3	8mA Pull-up	RST_OUT: watchdog reset signal output	VDDIO
PWRON	O	G1	8mA	PWRON: Power on/off control of main power	RTC_VDDIO
WKUP_PA30*	I	J1	8mA Schmitt	WKUP: Wakeup signal after main power down	RTC_VDDIO
PPRST_	I	J2	8mA Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	RTC_VDDIO
TEST_TE	I	L5	8mA Schmitt, Pull-down	TEST_TE: Manufacture test enable, program readable	RTC_VDDIO

Table 2-8 Boot Select Pins(2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PC00 (BOOT_SEL0)	IO I	D2	8mA Pullup-rst	PC00: GPIO group C bit 00 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PC01 (BOOT_SEL1)	IO I	D3	8mA Pulldown-rst	PC01: GPIO group C bit 01 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO

2.5.8 Digital IO/core power/ground

Table 2-9 IO/Core power supplies for FBGA (37)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO_D	P	N11,N12	-	VDDIO_D: IO digital power for power domain 0, 1.8V	-
VDDIO	P	N7,N8,N9,N10	-	VDDIO: IO digital power for power domain 1, 3.3V	-
VSS	P	J7,J8,J10,J11,J12,J13,K7,K8,K9,K10,K11,K12,K13,L8,L11	-	VSS: IO digital ground, include two power domain	-
VDD	P	J6,K6,L6,L7,L9,L10,L12,L13,M6,M7,M8,M9,M10,M11,M12,M13	-	VDD: 1.0V, CORE digital power	-

2.5.9 DDR power/ground

Table 2-10 DDR power/ground supplies Pins (35)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VREF	P	E5	-	VREF: DDR reference voltage, (VREF = VDDMEM/2)	-
VDDMEM	P	E6,E7,E8,E10,E11,E12,F5	-	VDDMEM: DDR IO supply(1.8V for DDR2)	-
VSSMEM	P	G5,G6,G7,G8,G9,G10,G11,G12	-	VSSMEM: DDR IO ground	-
DDRVDD	P	F6,F7,F8,F9,F10,F11,F12,F13	-	DDRVDD: DDR PHY 1.8V supply	-
DDRVSS	P	H6,H7,H8,H9,H10,H11,H12,H13	-	DDRVSS: DDR PHY ground	-
DDRPLL_AVD10	P	B9	-	DDRPLL_AVD10: DDR PLL 1.0V supply	-
DDRPLL_AVD18	P	E9	-	DDRPLL_AVD18: DDR PLL 1.8V supply	-
DDR_AVS	P	C9	-	DDR_AVS: DDR PLL analog ground	-

2.5.10 Analog - DDR

Table 2-11 DDR Analog Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DDR_ZQ	AIO	G13	-	DDR_ZQ: DDR2 External reference which is connected to a 240Ω resister to DDRVSS	VDDMEM

2.5.11 Analog - USB

Table 2-12 USB 2.0 OTG (8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB0PP	AIO	M2	-	USB0PP: USB data plus	USB_AVD33
USB0PN	AIO	N1	-	USB0PN: USB data minus	USB_AVD33
VBUS	AIO	P3	-	VBUS: The VBUS power supply can be used for a combination of functions. In the case of an un-powered device, it is used to supply current for driving the device, including the USB PHY. In the case of powered devices, it is also used for signaling to detect which device is connected. No charge pumps inside PHY, so no supplying capability by default. The PHY supports the VBUS divided to 3/5(default) off chip or not.	USB_AVD33
USB0ID	AI	N3	-	USB0ID: Used to identify the device attached to the PHY. The state of the pin is one if:high impedance(>1MΩ) or low impedance(<10Ω to ground).	USB_AVD18
USB_AVD33	P	M1	-	USB_AVD33: This is the analog supply that is used to support 3.3V signaling. This supply has both integrated IO pads and associated ESD. The expectation is that this supply is unique to the USB PHY. The PHY provides two pins for this power supply, but they can often be bonded out to a single package pin if the parasitic are low enough to support the current draw.	-
USB_AVD18	P	N2	-	USB_AVD18: This is the analog supply that is used to support 1.8V signaling. This supply has both integrated IO pads.	-
USB_AVD10	P	P2	-	USB_AVD10: This is the analog supply that is used to support 1.0V circuits within the PHY. This supply has both integrated IO pads and associated ESD. As this includes power supplied to the PLL and HS driver, the supply needs to be fairly quiet. The PHY provides two pins for this power supply, but they can often be bonded out to a single pin if the parasitic are low enough to support the current draw.	-
USB_AVS	P	N5	-	USB_AVS: This is the analog ground. This ground has both integrated IO pads and associated ESD. It is potentially sinking all the current accumulated for the PHY. The PHY provides two pins for this ground, but they can often be bonded out to a single pin if the ground lift can be kept less than 10mV.	-

2.5.12 Analog - SARADC

Table 2-13 SARADC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AUX0	AI	K3	-	AUX0: SARADC channel 0 input	SADC_AVD
AUX1	AI	L3	-	AUX1: SARADC channel 1 input	SADC_AVD
AUX2	AI	K2	-	AUX2: SARADC channel 2 input	SADC_AVD
SADC_AVD	P	L2	-	SADC_AVD: SARADC analog power, 1.8 V	-
SADC_AVS	P	M5	-	SADC_AVS: SARADC analog ground	-
SADC_VREF	P	L1	-	SADC_VREF: Voltage reference input, 0.5* SADC_AVD~0.99* SADC_AVD	-

2.5.13 Analog - CODEC

Table 2-14 CODEC Pins (7)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MICP	AI	R2	-	MICP: differential microphone input	CODEC_AVD
MICN	AI	R1	-	MICN: differential microphone input	CODEC_AVD
VCM	AO	T1	-	VCM: Reference voltage output	CODEC_AVD
MICBIAS	AO	R3	-	MICBIAS: Microphone bias output	CODEC_AVD
HPOUT	AO	U1	-	HPOUT: headphone output	CODEC_AVD
CODEC_AVD	P	T2	-	CODEC_AVD:1.8V analog supply	-
CODEC_AVS	P	N6	-	CODEC_AVS: analog ground	-

2.5.14 Analog - MIPI-CSI

Table 2-15 MIPI CSI(9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RX_DATAN0 (DVP_D0[1])	AIO	T16	-	RX_DATAN0(DVP_D0): Data lane 0 serial signal, reused with DVP data bit 0 input signal	CSI_AVDx[2]
RX_DATAP0 (DVP_D1)	AIO	U17	-	RX_DATAP0(DVP_D1): Data lane 0 serial signal, reused with DVP data bit 1 input signal	CSI_AVDx
RX_DATAN1 (DVP_D2)	AIO	R17	-	RX_DATAN1(DVP_D2): Data lane 1 serial signal, reused with DVP data bit 2 input signal	CSI_AVDx
RX_DATAP1 (DVP_D3)	AIO	P15	-	RX_DATAP1(DVP_D3): Data lane 1 serial signal, reused with DVP data bit 3 input signal	CSI_AVDx
RX_CLKN (DVP_D4)	AIO	T17	-	RX_CLKN(DVP_D4): Clock lane serial signal, reused with DVP data bit 4 input signal	CSI_AVDx
RX_CLKP (DVP_D5)	AIO	R16	-	RX_CLKP(DVP_D5): Clock lane serial signal, reused with DVP data bit 5 input signal	CSI_AVDx
CSI_AVD10	P	R14	-	CSI_AVD10: PHY analog power, 1.0V	-
CSI_AVD18	P	R15	-	CSI_AVD18: PHY analog power, 1.8V	-

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CSI_AVS	P	N13	-	CSI_AVS: PHY analog ground	-

NOTES:

1. DVP signals can input form this Pad when change the configure in controller
2. CSI_AVDx: means MIPI-CSI IO Pad interface support two power supply(TTL and CMOS)

2.5.15 Analog - EFUSE

Table 2-16 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	K5	-	AVDEFUSE: EFUSE programming power, 0V/1.5V	-

2.5.16 Analog - CLOCK/PLL

Table 2-17 CLOCK/PLL Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	F2	2~30 MHz Oscillator, OSC on/off	EXCLK_XI: external oscillator clock input or external 24MHz clock input	VDD
EXCLK_XO	AO	F1		EXCLK_XO: external oscillator clock output	VDD
PLL0_VDDA	P	E2	-	PLL0_VDDA: PLL analog power, 1.8V	-
PLL0_VSSA	P	H5	-	PLL0_VSSA: PLL analog ground	-
PLL1_VDDA	P	E1	-	PLL1_VDDA: PLL analog power, 1.8V	-
PLL1_VSSA	P	J5	-	PLL1_VSSA: PLL analog ground	-

2.5.17 Analog - RTC

Table 2-18 RTC Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
osc32_XI	AI	H3	32.768KHz Oscillator	osc32_XI: 32.768KHz clock input	RTC_VDDIO
osc32_XO	AO	H2		osc32_XO: Reserved	RTC_VDDIO
RTC_VDD	P	G2	-	RTC_VDD: 1.0V power for RTC	-
RTC_VDDIO	P	J3	-	RTC_VDDIO: 3.3V power for RTC	-

NOTES:

1 All GPIO are programmable with multi-voltage (1.8V, 2.5V, 2.8V. 3.0V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

2 The meaning of phases in IO cell characteristics are:

- 8/16mA: The IO cell's output driving strength is about 8/16mA.
- Pull-up: The IO cell contains a pull-up resistor and fixed pull up.
- Pull-down: The IO cell contains a pull-down resistor and fixed pull down.
- Pullup-rst: The IO cell during reset and after the pull up function is enabled.
- Pulldown-rst: The IO cell during reset and after the pull down function is enabled.
- Schmitt: The IO cell is Schmitt trigger input and fixed.
- Schmitt-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
- Slew-rate-rst: The IO cell during reset and after the slew-rate function select fast mode.

3 *: This pin has GPIO function as group A bit 30, but only input/interrupt function.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.1	1.98	V
DDRVDD power supplies voltage	-0.1	1.65	V
DDRPLL_AVD18 power supplies voltage	-0.1	1.98	V
DDRPLL_AVD10 power supplies voltage	-0.1	1.1	V
VDDIO power supplies voltage	-0.5	3.63	V
VDDIO_D power supplies voltage	-0.5	3.63	V
VDD power supplies voltage	-0.2	1.1	V
PLL0_VDDA power supplies voltage	-0.1	1.98	V
PLL1_VDDA power supplies voltage	-0.1	1.98	V
AVDEFUSE power supplies voltage	-0.1	1.65	V
RTC_VDD power supplies voltage	-0.5	1.155	V
RTC_VDDIO power supplies voltage	-0.5	3.63	V
USB_AVD33 power supplies voltage	-0.1	3.63	V
USB_AVD18 power supplies voltage	-0.1	1.98	V
USB_AVD10 power supplies voltage	-0.1	1.1	V
SADC_AVD power supplies voltage	-0.1	1.98	V
CODEC_AVD power supplies voltage	-0.1	1.98	V
CSI_AVD10 power supplies voltage	-0.1	1.1	V
CSI_AVD18 power supplies voltage	-0.1	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VDDMEM	VDDMEM voltage for SSTL18 (DDR2)	1.62	1.8	1.98	V

DDRVDD	DDR PHY power supplies voltage	1.35	1.5	1.65	V
DDRPLL_AVD18	DDR PLL power supplies voltage	1.62	1.8	1.98	V
DDRPLL_AVD10	DDR PLL power supplies voltage	0.9	1.0	1.1	V
VDDIO	GPIO power domain 1 supplies voltage	1.5	3.3	3.63	V
VDDIO_D	GPIO power domain 2 supplies voltage	1.62	1.8	1.98	V
VDD	VDD core supplies voltage	0.9	1.0	1.1	V
PLL0_AVD	VPLL and MPLL analog voltage	1.62	1.8	1.98	V
PLL1_AVD	APLL and EPLL analog voltage	1.62	1.8	1.98	V
AVDEFUSE	EFUSE program supplies voltage	1.35	1.5	1.65	V
RTC_VDD	RTC core supplies voltage	0.72	1.0	1.155	V
RTC_VDDIO	RTC IO supplies voltage	1.35	3.3	3.63	V
USB_AVD33	USB PHY VCCA3P3 analog voltage	3.0	3.3	3.6	V
USB_AVD18	USB PHY VCC18 analog voltage	1.62	1.8	1.98	V
USB_AVD10	USB PHY VCCCORE1P0 voltage	0.9	1.0	1.1	V
SADC_AVD	SAR-ADC analog voltage	1.62	1.8	1.98	V
CODEC_AVD	CODEC analog voltage	1.62	1.8	1.98	V
CSI_AVD10	MIPI PHY 1.0V analog voltage	0.9	1.0	1.1	V
CSI_AVD18	MIPI PHY 1.8V analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO/VDDIO_D/RTC_VDDIO supplied pins

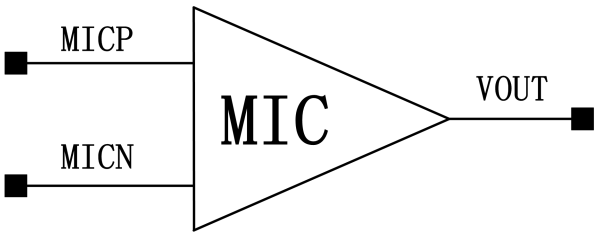
Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	*0.65	-	+0.3	V
V_{IL18}	Input low voltage for 1.8V I/O application	-0.3	-	*0.35	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7	-	+0.3	V
V_{IL25}	Input low voltage for 2.5V I/O application	-0.3	-	0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2	-	+0.3	V
V_{IL33}	Input low voltage for 3.3V I/O application	-0.3	-	0.8	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	-40	25	+125	°C

3.3 Audio codec

3.3.1 Microphone input

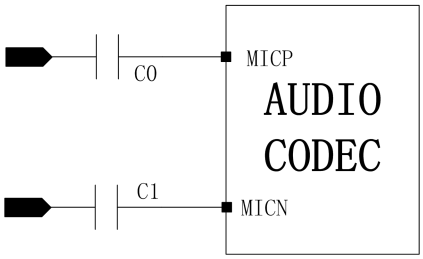


There are two microphone input channels, MICP and MICN. They can be configured as differential inputs by the microphone PGA(MIC).

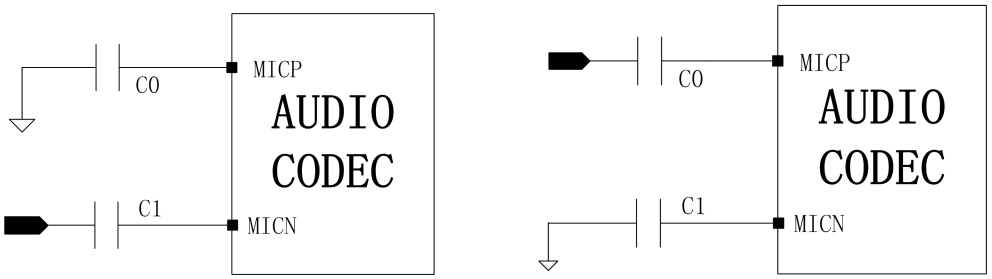
The signal of microphone output should be input to AUDIO CODEC through DC-blocking capacitor, as shown in following figure. The capacitance and input resistance form a high pass filter. For example, when the gain of the MIC module is 20dB, the input resistance is 45KΩ and 0.1uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 45 \times 10^{3} \times 0.1 \times 10^{-6}} = 35.4Hz$$

The capacitance of the DC-blocking capacitor should be determined by the minimum input impedance and application requirements.



If the output of microphone is single-ended, the AUDIO ADC input should be connected as following figure.



Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

3.3.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

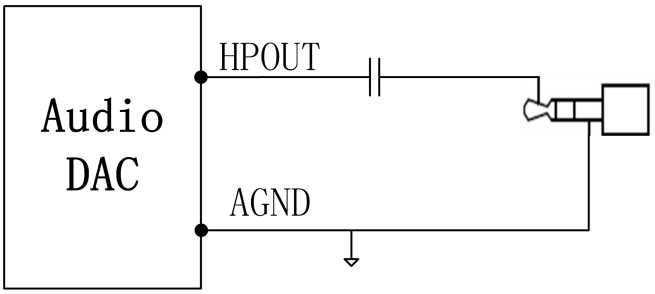
3.3.3 Headphone output

Audio codec DAC output can drive 16Ω or 32Ω headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16 Ω headphone and 100uF DC-blocking capacitor are used, the lower cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

3.3.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.8*CODEC_AVD to 0.975* CODEC_AVD with a step of 0.025* CODEC_AVD.

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1830 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-5 gives the timing parameters. Following are the name of the power.

- VDDRTC: RTC_VDDIO, RTC_VDD
- AVDAUD: CODEC_AVD
- VDD10: all 1.0V power supplies, include VDD
- VDD: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIO_D
- AVD: all other analog power supplies: SADC_AVDD, USB_AVD33, USB_AVD18, USB_AVD10, PLL0_AVD, PLL1_AVD, CSI_AVD18, CSI_AVD10

Table 3-5 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD10}	VDD10 rise time[1]	0	5	ms
t_{D_VDD10}	Delay between VDD arriving 50% (or 90%) to VDD10 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD10 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]

NOTES:

- The power rise time is defined as 10% to 90%.
- The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

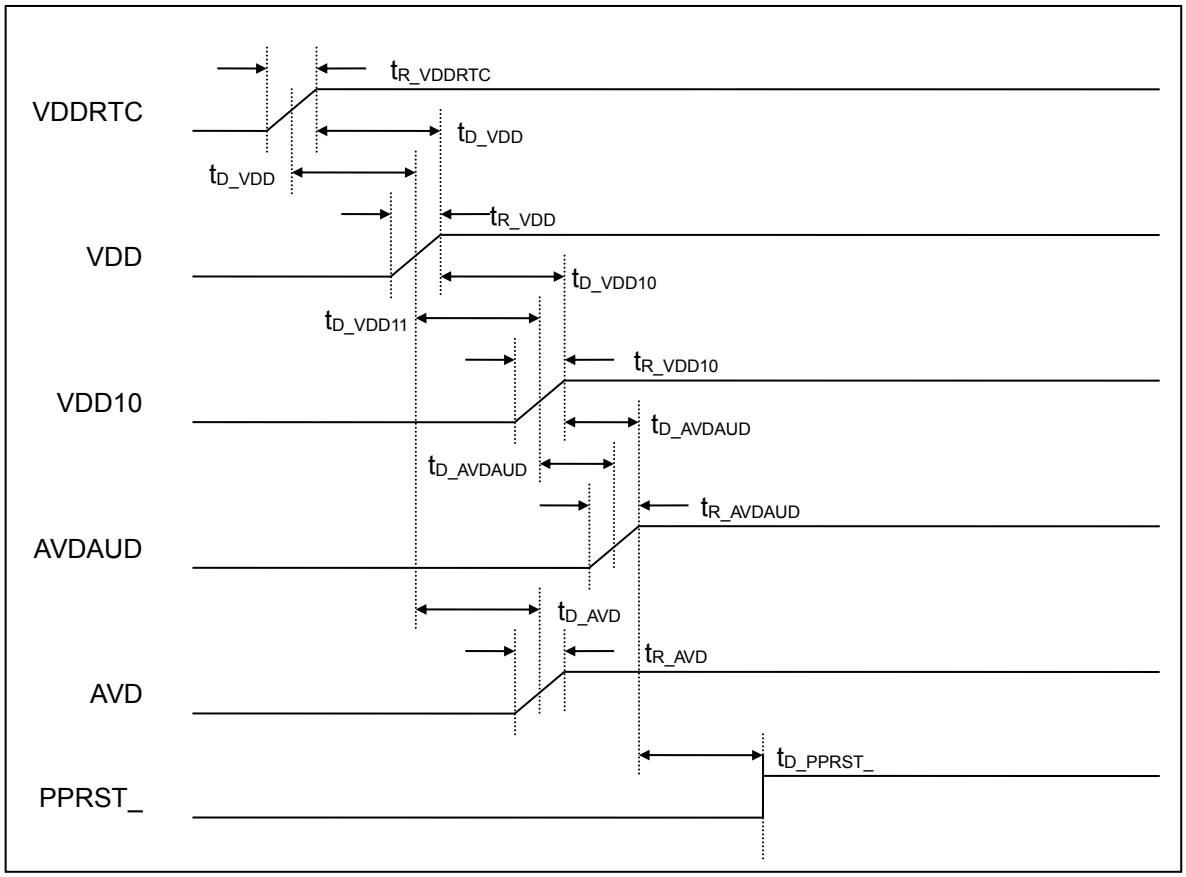


Figure 3-1 Power-On Timing Diagram

3.4.2 Reset procedure

There are 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

- PPRST_ pin reset.
  This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
- WDT reset.
  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
- Hibernating reset.
  This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description [1][2]” for details. The PWRON is output 1. The oscillators

are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.4.3 BOOT

The boot sequence of the X1830 is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 3-6 Boot Configuration of X1830

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot)
10	NOR boot @ CS2 (just for FPGA testing)
11	USB boot @ USB 2.0 device, EXTCLK=24MHz

The boot procedure is showed in the following flow chart:

As shown in Figure 3-2 boot sequence Block Diagram， after reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[1:0] to determine the boot method.
2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.
3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.
4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.
5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the 12kB code from SPI NAND/NOR flash to cache and jump to it.
6 If it is boot from NOR Flash, the boot program jump to nor and run directory.

When SFC boot start failure, the program in bootrom will go into MSC0 boot, If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.

When MSC0 boot start failure, the program in bootrom will go into MSC1 boot， If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the 26KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.If MSC1 boot start failure, jump to USB boot.

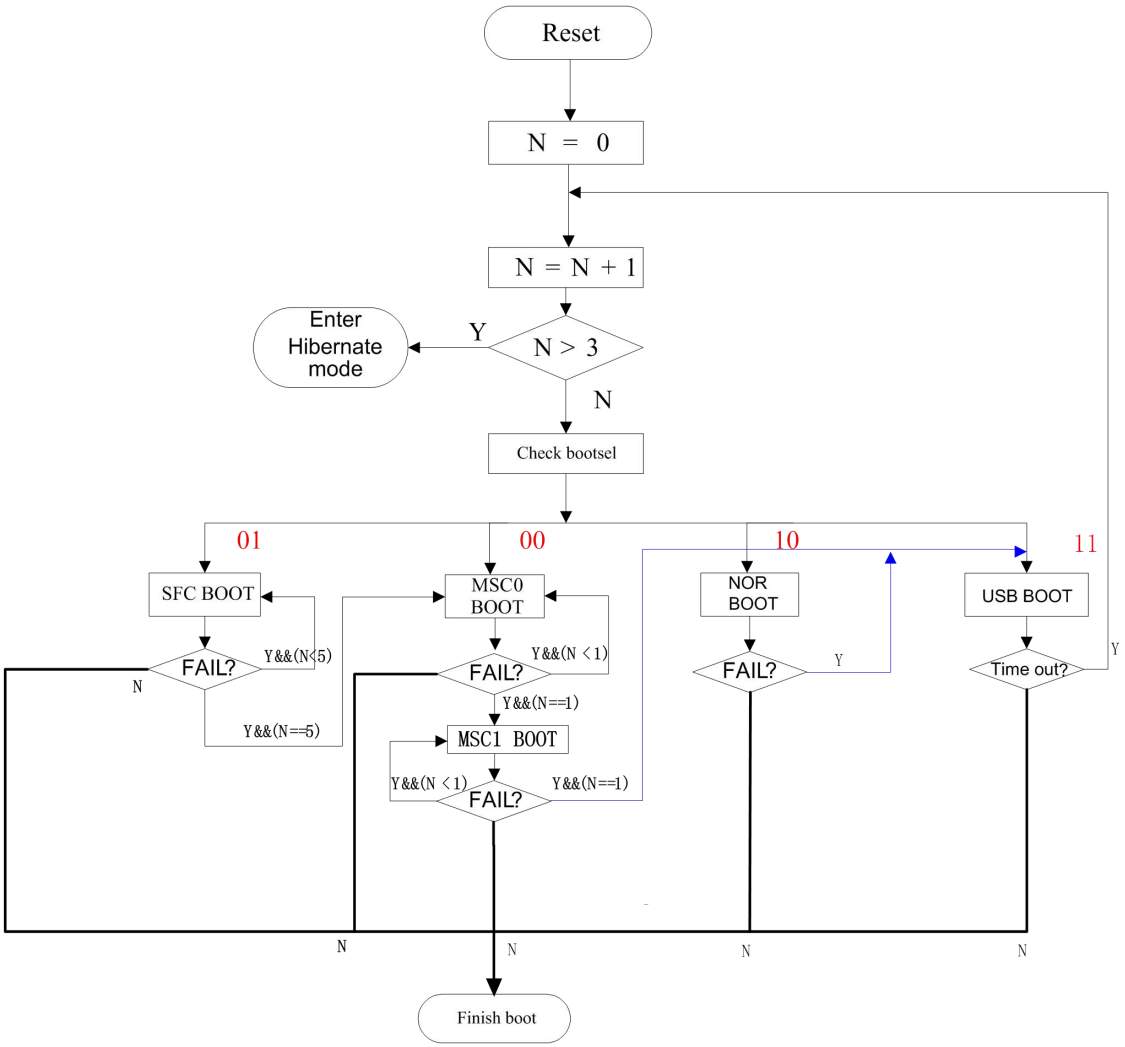


Figure 3-2 Boot sequence diagram of X1830